AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An electronic circuit comprising:

a central processing unit having a clock connection for receiving a first clock and a data connection;

a peripheral unit having a clock connection and a data connection, said clock connection being connected to a signal output of a controllable oscillator or to an external clock input, so that the peripheral unit receives a second clock which is different from ~~relatively prime with respect to~~ the first clock and whose clock frequency is relatively prime with respect to ~~has no common divisor with~~ the first clock;

synchronization means comprising a first and a second data connection, said first data connection being connected to said data connection of said peripheral unit; and

a data bus being connected to said data connection of said central processing unit and to said second data connection of said synchronization means.

2. (Original) The electronic circuit according to claim 1, wherein said central processing unit, said peripheral unit, said synchronization means and said data bus are arranged on a common chip card having two external connection devices being arranged to be connectable to two corresponding contact connections of a terminal, a first of said contact connections being connected to said signal output of said controllable oscillator, a clock signal for said central processing unit being applied at the second of said contact connections, a first of said external connection devices being connected to said clock connection of said peripheral unit and the second of said external connection devices being connected to said clock connection of said central processing unit.

3. (Original) The electronic circuit according to claim 1, wherein said central processing unit, said peripheral unit, said synchronization means, said data bus

and said oscillator are arranged on a common chip card, and wherein said clock connection of said peripheral unit is connected to said signal output of said controllable oscillator.

4. (Original) The electronic circuit according to claims 1, wherein said central processing unit, said peripheral unit, said data bus, said controllable oscillator and said synchronization means are integrated into an integrated circuit.

5. (Original) The electronic circuit according to claim 1, further comprising: controlling means having a control output, said control output being connected to said control input of said controllable oscillator, and said controlling means being arranged to control said controllable oscillator depending on a control parameter.

6. (Original) The electronic circuit according to claim 5, wherein said controlling means is arranged to control said controllable oscillator as a control parameter depending on a task performed by said peripheral unit, an application of said electronic circuit or energy available for said electronic circuit.

7. (Original) The electronic circuit according to claim 1, wherein said controllable oscillator is controllable to provide an output signal at a signal output, the frequency of which is faster than a frequency of a clock signal which can be fed to said clock connection of said central processing unit.

8. (Original) The electronic circuit according to claim 1, wherein said controllable oscillator is controllable to provide an output signal, the frequency of which has no common divisor with a frequency of a clock signal which can be fed to said clock connection of said central processing unit.

9. (Original) The electronic circuit according to claim 1, being embodied as a cryptography controller.

10. (Original) The electronic circuit according to claim 1, wherein said peripheral unit is a coprocessor for one of a group of cryptographic algorithms including an asymmetrical encrypting or a symmetrical encrypting, a transceiver, a filter, a hash module, a random generator or a sensor element.

11. (Original) The electronic circuit according to claim 1, comprising a plurality of peripheral units, each peripheral unit being connectable to a separate controllable oscillator, or wherein clock signals with frequencies are fed to various of said plurality of peripheral units, these frequencies being derived from said controllable oscillator.

12. (Currently Amended) The electronic circuit according to claim [[1]] 11, wherein a separate task is associated to each peripheral unit, the tasks being selected from a group including computing a modular multiplication, a modular addition, a hash value computation, an RSA encrypting, an encrypting based on elliptical curves, an encrypting according to the DES standard, a data exchange with a terminal, forming random numbers or checking safety-critical parameters.

13. (Original) A method of controlling an electronic circuit having a central processing unit (CPU) and a peripheral unit being connected to each other via a data bus, comprising: clocking said central processing unit by a first clock; clocking said peripheral unit by a second clock which is different from the first clock, so that the clock frequency of the second clock is relatively prime with respect to the clock frequency of the first clock; and synchronizing data transmitted between said central processing unit and said peripheral unit via said data bus.

14. (New) The electronic circuit according to claim 1, wherein said clock connection is connected to the signal output of the controllable oscillator or to the external clock input, so that the second clock is — irrespective of the unit used for

representing the frequencies of the first and the second clocks — relatively prime with respect to the first clock.

15. (New) An electronic circuit comprising:

a central processing unit having a clock connection for receiving a first clock and a data connection;

a peripheral unit having a clock connection and a data connection, said clock connection being connected to a signal output of a controllable oscillator so that the peripheral unit receives a second clock which is different from the first clock and whose clock frequency is relatively prime with respect to the first clock;

synchronization means comprising a first and a second data connection, said first data connection being connected to said data connection of said peripheral unit; and

a data bus being connected to said data connection of said central processing unit and to said second data connection of said synchronization means.

16. (New) An electronic circuit comprising:

a central processing unit having a clock connection for receiving a first clock and a data connection;

a peripheral unit having a clock connection and a data connection, said clock connection being connected to a signal output of a controllable oscillator or to an external clock input, so that the peripheral unit receives a second clock which is different from the first clock and whose clock frequency is independent from the first clock;

synchronization means comprising a first and a second data connection, said first data connection being connected to said data connection of said peripheral unit; and

a data bus being connected to said data connection of said central processing unit and to said second data connection of said synchronization means.

17. (New) A method of controlling an electronic circuit having a central processing unit (CPU) and a peripheral unit being connected to each other via a data bus, comprising:

clocking said central processing unit by a first clock;

clocking said peripheral unit by a second clock which is different from the first clock, so that the clock frequency of the second clock is independent from the clock frequency of the first clock; and

synchronizing data transmitted between said central processing unit and said peripheral unit via said data bus.